Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A magnetic memory device, comprising:

a plurality of magnetoresistive devices including a magnetic sensitive layer of which the magnetization direction changes according to an external magnetic field;

a plurality of write lines where a write current for generating an external magnetic field which is applied to the magnetic sensitive layer flows;

a plurality of current direction control circuits each of which is disposed for each write line, and has a function of controlling the direction of a write current in each write line according to an inputted write data signal; and

a constant current circuit being shared among the plurality of current direction control circuits and making the write current flowing through each write line ~~constant.~~constant, wherein

each write line has a loop shape in which both ends of the write line are connected to the current direction control circuit.

2. (Canceled).

3. (Original) A magnetic memory device according to claim 1, wherein

the current direction control circuit includes:

a first differential switch pair including a first current switch and a second current switch which are disposed corresponding to both ends of the write line, and operate to turn to switching states different from each other;

a second differential switch pair including a third current switch and a fourth current switch which are disposed corresponding to the first current switch and the second

current switch, respectively, and operate to turn to switching states different from each other; and

a differential control means including a fifth current switch and a sixth current switch which operate to turn to switching states different from each other, and controlling to bring the first current switch and the fourth current switch into the same switching state and bring the second current switch and the third current switch into a switching state different from that of the first current switch and the fourth current switch.

4. (Original) A magnetic memory device according to claim 3, wherein

the first through sixth current switches include first through sixth transistors, respectively.

5. (Original) A magnetic memory device according to claim 4, further comprising:

a circuit selector switch for each current direction control circuit so as to select one of a plurality of current direction control circuits,

wherein the constant current circuit includes:

a resistor for current control; and

a transistor for current control in which the collector terminal thereof is commonly wired to the emitter terminals of the third transistors and the fourth transistors in the plurality of current direction control circuits through the circuit selector switch, and the emitter terminal thereof is grounded through the resistor for current control, and a constant voltage is selectively inputted into the base terminal thereof, and

the sum of currents flowing through the third transistor and the fourth transistor in a current direction control circuit selected by the circuit selector switch becomes constant by the constant current circuit.

6. (Original) A magnetic memory device according to claim 5, wherein

the constant voltage is produced through the use of a band gap reference.

7. (Original) A magnetic memory device according to claim 5, wherein

a diode is disposed between the base of the transistor for current control and the ground.

8. (Original) A magnetic memory device according to claim 5, wherein

the switching operation of the circuit selector switch is controlled on the basis of a circuit selection signal for selecting one of the plurality of current direction control circuits.

9. (Original) A magnetic memory device according to claim 5, wherein

the switching operation of the circuit selector switch is controlled on the basis of a circuit selection signal for selecting one of the plurality of current direction control circuit and a write selection signal indicating a write mode.

10. (Original) A magnetic memory device according to claim 4, wherein

the base terminal of the fifth transistor is connected to the collector terminal of the third transistor, and the collector terminal of the fifth transistor is connected to the base terminal of the second transistor, and

the base terminal of the sixth transistor is connected to the collector terminal of the fourth transistor, and the collector terminal of the sixth transistor is connected to the base terminal of the first transistor.

11. (Original) A magnetic memory device according to claim 4, further comprising:

a second constant current circuit being shared among the plurality of current direction control circuits, and making the sum of currents flowing through the fifth transistor and the sixth transistor constant.

12. (Original) A magnetic memory device according to claim 11, further comprising:

a second circuit selector switch for each current direction control circuit so as to select one of a plurality of current direction control circuits,

wherein the second constant current circuit includes:

a second resistor for current control; and

a second transistor for current control in which the collector terminal thereof is commonly wired to the emitter terminals of the fifth transistors and the sixth transistors in the plurality of current direction control circuits through the second circuit selector switch, and the emitter terminal thereof is grounded through the second resistor for current control, and a constant voltage is selectively inputted into the base terminal thereof.

13. (Original) A magnetic memory device according to claim 4, wherein

the collector terminals of the first transistor and the second transistor are connected to a power source,

an end of the write line is connected to the emitter terminal of the first transistor and the collector terminal of the third transistor, and

the other end of the write line is connected to the emitter terminal of the second transistor and the collector terminal of the fourth transistor.

14. (Original) A magnetic memory device according to claim 4, wherein

the data signal is inputted into the base terminal of either the third transistor or the fourth transistor, and an inversion signal of the data signal is inputted into the base terminal of the other transistor.

15. (Original) A magnetic memory device according to claim 4, wherein

the fifth transistor detects the switching state of the third transistor, and operates the second transistor to turn to the same switching state as that of the third transistor, and

the sixth transistor detects the switching state of the fourth transistor, and operates the first transistor to turn to the same switching state as that of the fourth transistor.

16. (Original) A magnetic memory device according to claim 4, wherein

a first bias resistor is disposed between a connection point of the collector terminal of the fifth transistor and the base terminal of the second transistor and a power source, and

a second bias resistor is disposed between a connection point of the collector terminal of the sixth transistor and the base terminal of the first transistor and the power source.

17. (Original) A magnetic memory device according to claim 1, wherein

the magnetoresistive device includes:

a laminate which includes the magnetic sensitive layer and through which a current flows in a direction perpendicular to a laminate surface; and

a toroidal magnetic layer which is disposed on one surface of the laminate so that its direction along the laminate surface is its axial direction, and the write line passes through the toroidal magnetic layer.

18. (Original) A magnetic memory device according to claim 17, wherein

the write line includes a plurality of first write lines and a plurality of second write lines extending so as to intersect with the plurality of first write lines, and

the first write lines and the second write lines extend in parallel to each other in a region where the first write lines and the second write lines pass through the toroidal magnetic layer.

19. (Original) A magnetic memory device according to claim 1, wherein one memory cell includes a pair of the magnetoresistive devices.

20. (Currently Amended) A magnetic memory device according to claim 19, wherein

the magnetization directions of magnetic sensitive layers in the pair of magnetoresistive devices change according to a magnetic field induced by a current flowing through ~~the first~~ a first write line ~~and the~~ and a second write line so as to be antiparallel to each other, thereby information is stored in the memory cell.

21. (Original) A write current drive circuit, being applied to a magnetic memory device, the magnetic memory device including a plurality of magnetoresistive devices including a magnetic sensitive layer of which the magnetization direction changes according to an external magnetic field, and a plurality of loop-shaped write lines where a write current for generating an external magnetic field which is applied to the magnetic sensitive layer flows, the write current drive circuit comprising:

a pair of connection ends to which both ends of the write line are connected;

a plurality of current direction control circuits each of which is disposed for each write line, and has a function of controlling the direction of a write current in each write line according to an inputted write data signal; and

a constant current circuit being shared among the plurality of the current direction control circuits, and making the write current flowing through each write line constant.

22. (Original) A write current driving method, being applied to a magnetic memory device, the magnetic memory device including a plurality of magnetoresistive devices including a magnetic sensitive layer of which the magnetization direction changes according to an external magnetic field, and a plurality of loop-shaped write lines where a

write current for generating an external magnetic field which is applied to the magnetic sensitive layer flows,

wherein a current direction control circuit is disposed for each write line, and both ends of the write line are connected to the current direction control circuit, and a constant current circuit is shared among the plurality of current direction control circuits, and

the current direction control circuit controls the direction of a write current in each write line according to an inputted write data signal, and the constant current circuit makes the write current flowing through each write line constant.